REMARKS

Upon entry of this Response, claims 1, 8, 16, and 21 will be amended and claims 3-4, 10, 13, and 18-20 will be canceled. No new matter has been added. Reconsideration and further examination are respectfully requested.

New Claim Rejections – 35 USC § 112, 2nd Paragraph

Claims 1-2, 5-9, and 11-24 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims have been amended in view of the Examiner's helpful comments.

New Claim Rejections – 35 USC § 102(e)

Claims 1-2, 5-9, 11, and 13-20 are rejected as being anticipated by U.S. Patent No. 6,789,140 ("Kotani").

As amended, claim 1 recites retrieving an instruction via an n-bit input path, pre-decoding the instruction at a Direct Memory Access (DMA) unit, and providing the pre-decoded instruction from the DMA unit to a processing unit via a q-bit output path (where $n < q$). The instruction may then be decoded and executed at the processing unit.

The references fail to disclose or suggest such a feature. According to the Office Action[1], it is

> inherent [in Kotani] that the output path from the DMA must be larger [than the input path] to be able to send out the control signals to the host processor when an interrupt is detected.

(Office Action, page 5-6 paragraph 20). However, as amended claim 1 now recites that the processing element decodes the pre-decoded instruction received via the q-bit output path. Such an arrangement is not disclosed or suggested by Kotani. For example, as illustrated in FIG. 9 of Kotani a DMA controller 234 may provide Interrupt Signal (IS) information to a host CPU 210

[1] The section of the Office Action relates to previously pending claim 18, which contains similar limitation to those found in claim 1 as amended.

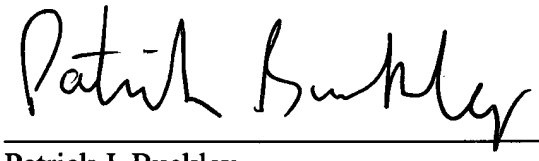
that does not decode the instruction and Run Signal (RS) information to a drawing section 232. Thus, the reference does not disclose an n-bit input path and a q-bit output path to a processing unit that decodes an instruction where $n < q$. Applicants respectfully request allowance of claim 1.

Remaining claims depend from claim 1 (or contain similar limitations) and should therefore also be allowable.

CONCLUSION

Accordingly, Applicants respectfully request allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-0191.

Respectfully submitted,



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